

ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor device has a memory cell array having electrically erasable programmable non-volatile memory cells, reprogramming and retrieval circuits that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array. Each reprogramming and retrieval circuit has a first latch and a second latch that are selectively connected to the memory cell array and transfer data each other. A controller controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array. Each reprogramming and retrieval circuit has a multilevel logical operation mode and a caching operation mode. In the multilevel logical operation mode, re-programming and retrieval of upper and lower bits of two-bit four-level data is performed using the first and the second latches in storing the two-bit four-level data in one of the memory cells in a predetermined threshold level range. In the caching operation mode, data transfer between one of the memory cells selected in accordance with a first address and the first latch is performed while data transfer is performed between the second latch and input/output terminals in accordance with a second address with respect to one-bit two-level data to be stored in one of the memory cells.